

Figure 12:

GX Packet Format  
(n=4)

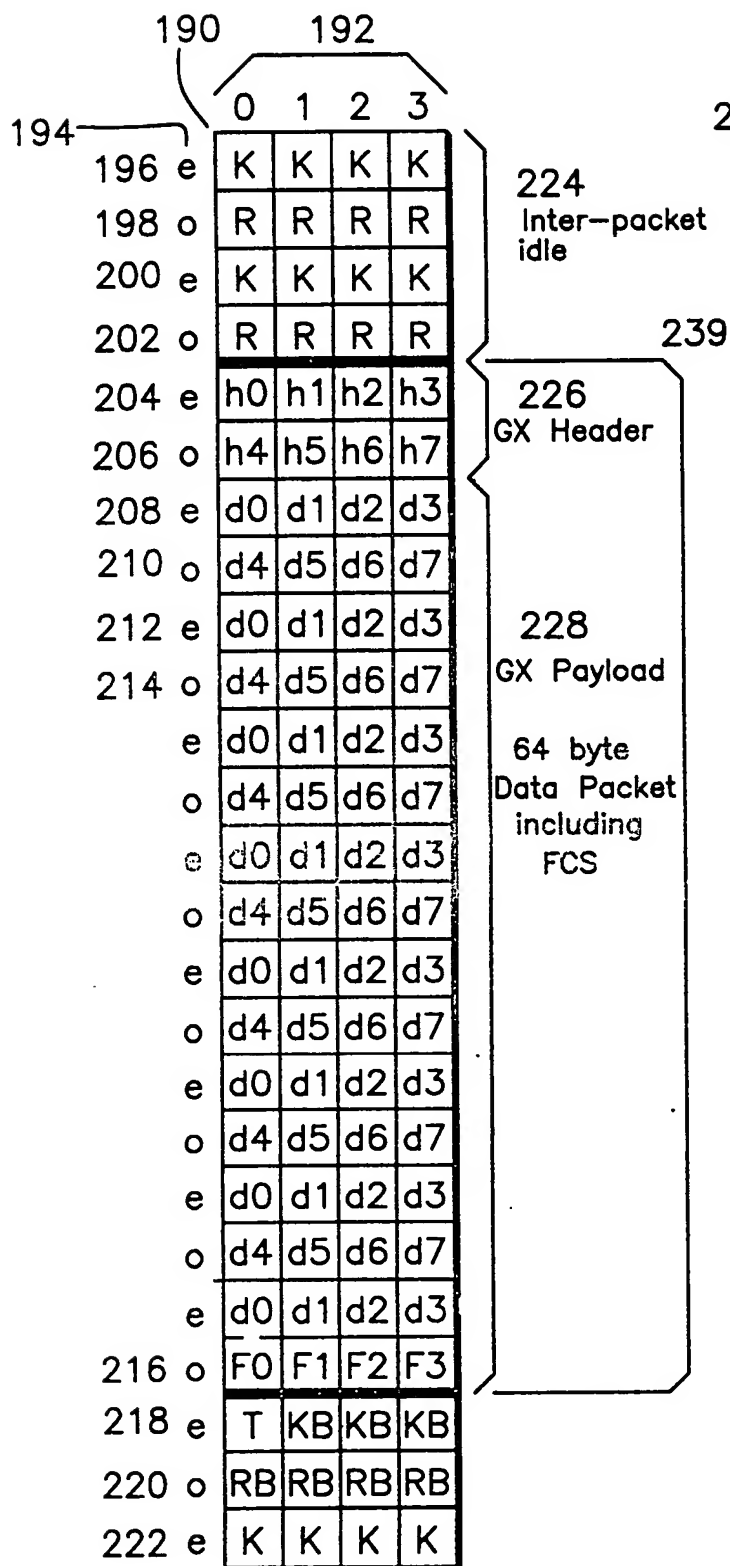
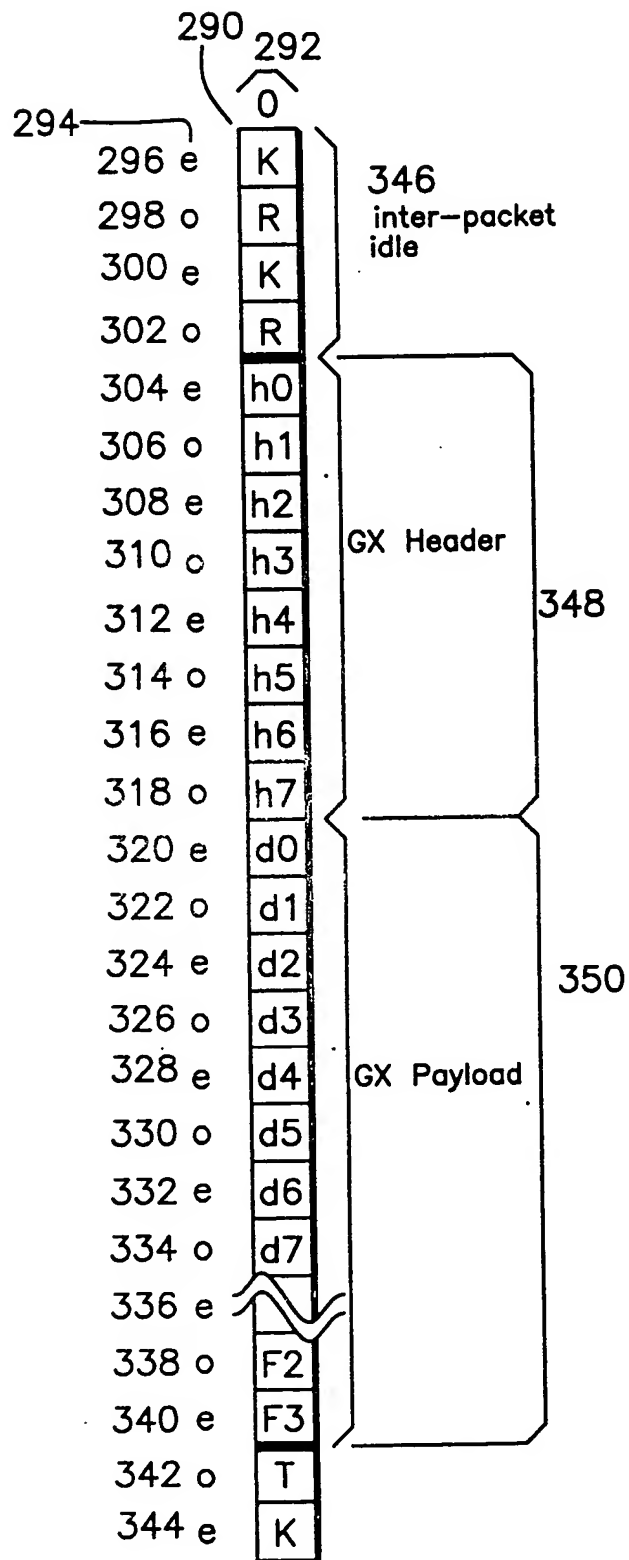


Figure 14:  
GX Packet Format (n=1)



Transmit Processor  
(n=8)

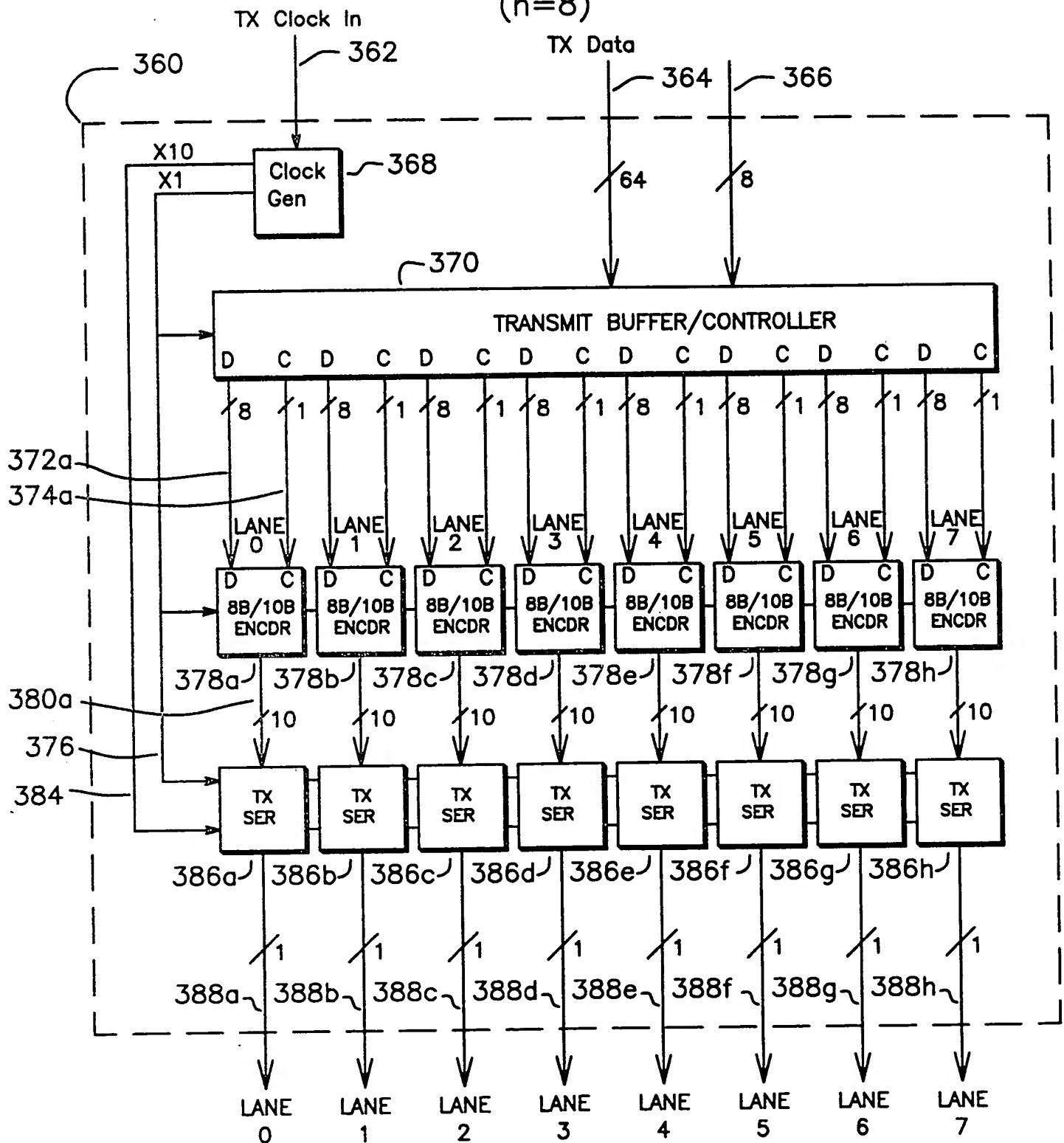


Figure 16:  
Transmit Processor (n=4)

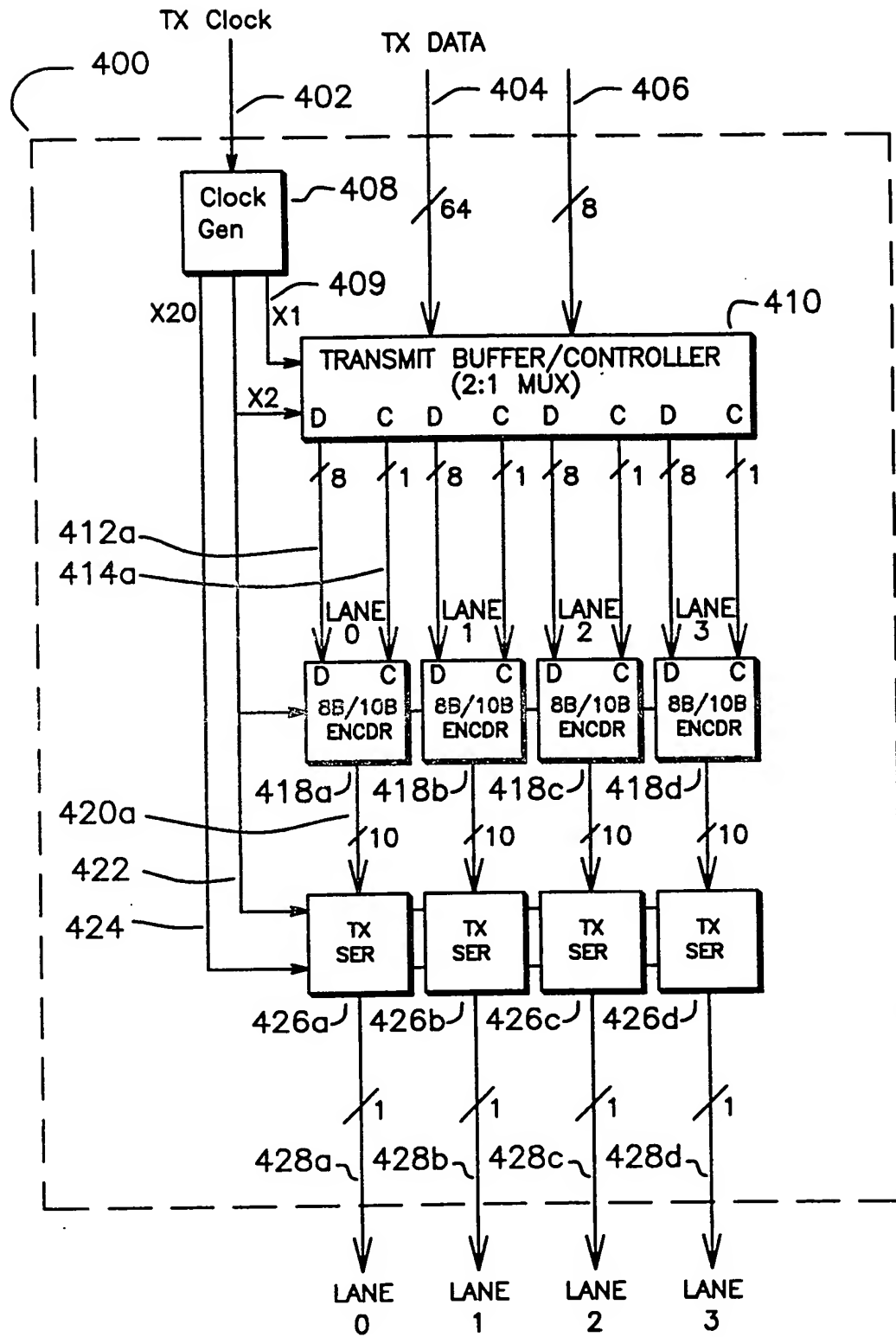


Figure 17a:  
8B/10B Encoder

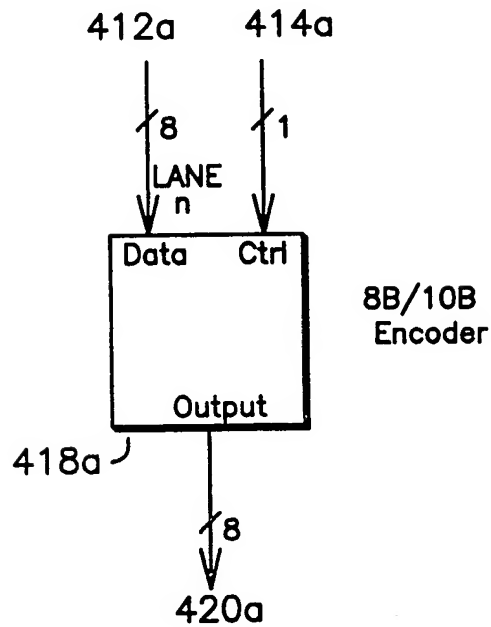


Figure 17b:  
8B/10B Encoder

	8B Input	Ctrl Input	10B Output
440	START	CTRL	Start
442	8B_Data	DATA	10B_Data
444	END	CTRL	End
446	IDLE-EVEN	CTRL	Even_Idle
448	IDLE-ODD	CTRL	Odd_Idle
449	IDLE-EVEN_BUSY	CTRL	Even_Idle_Busy
450	IDLE-ODD_BUSY	CTRL	Odd_Idle_Busy



Figure 18:  
Receive Processor (n=8)

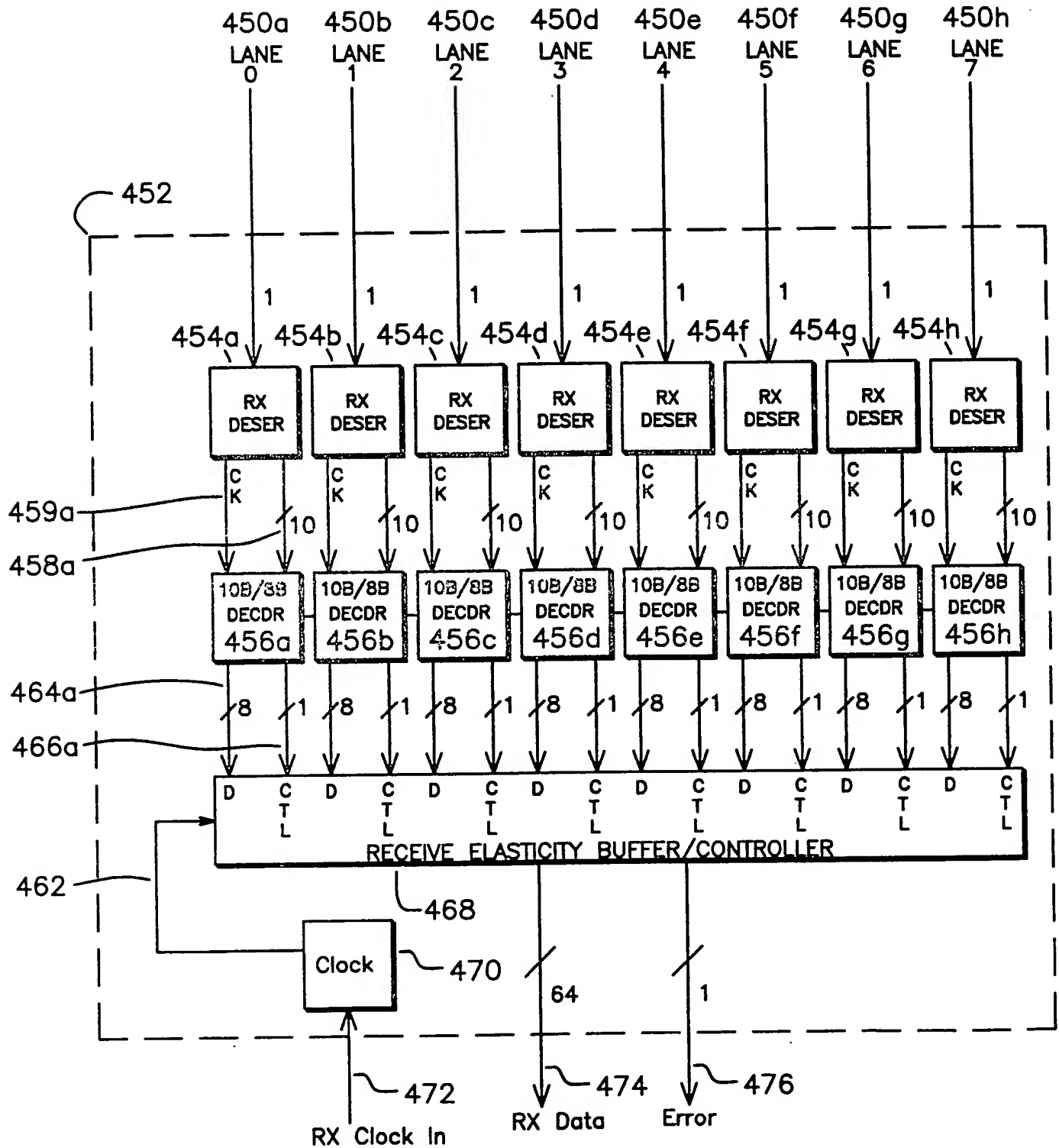


Figure 19:  
Receive Processor (n=4)

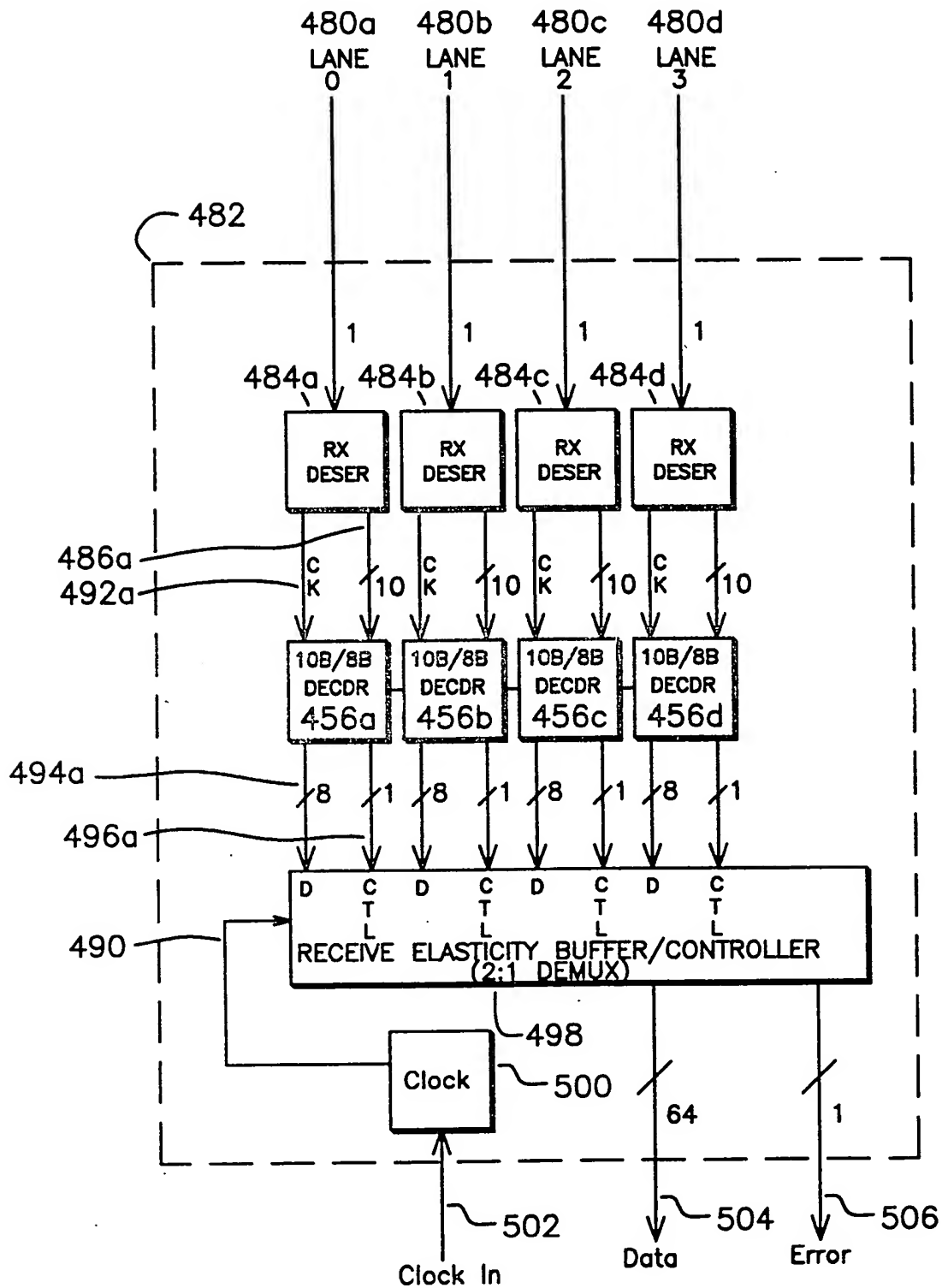


Figure 20a:  
10B/8B Decoder

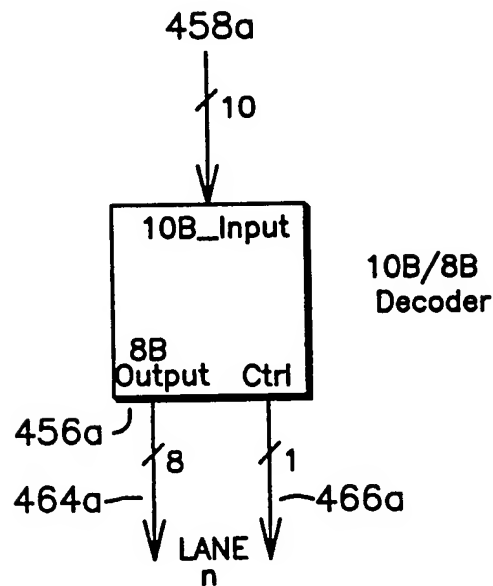


Figure 20b:  
10B/8B Decoder

	10B Input	8B Output	Ctrl Output
470	Start	START	CTRL
472	10B_Data	8B_Data	DATA
474	End	END	CTRL
476	Even_Idle	IDLE-EVEN	CTRL
478	Odd_Idle	IDLE-ODD	CTRL
480	Even_Idle_Busy	IDLE-EVEN-BUSY	CTRL
482	Odd_Idle_Busy	IDLE-ODD-BUSY	CTRL